REMARKS

Claims 1-30 are pending. Claims 1, 14, 21, 29, and 30 are independent claims. Claims 1, 14, 21, 29, and 30 are amended in this response. No new matter is added. Favorable reconsideration and allowance of the above-referenced application are respectfully requested.

35 USC 101

Claims 1, 14, 21, 29, and 30 stand rejected under 35 USC 101 as allegedly being directed to non-statutory subject matter.

As amended, claim 1 recites, "pushing a datum onto a stack by a first hardware-controlled processing thread in a hardware-based multi-threaded processor to make available the datum for other hardware-controlled processing threads in the hardware-based multi-threaded processor, the processing thread comprising computer instructions that perform a task; and popping the datum off the stack by a second hardware-controlled processing thread in the hardware-based multi-threaded processor to use the datum, the second processing thread comprising computer instructions that perform a task." (Emphasis added).

The practical application of pushing a datum onto a stack by a first processing thread is to make available the datum for other processing threads. Similarly, the practical application

of popping the datum from the stack by a second processing thread is to use the datum. Accordingly, it is respectfully requested that the rejection of claim 1 under 35 USC 101 be withdrawn. The rejections of claims 14 and 30 under 35 USC 101 should also be withdrawn for reasons similar to claim 1 and the additional recitations that they contain.

As amended, claim 21 recites, "control logic that responds to commands from at least two hardware-controlled processing threads in a hardware-based multi-threaded processor, the control logic storing datum on a stack structure in response to a push command to make available the datum for other hardware-controlled processing threads in the hardware-based multi-threaded processor and retrieving datum to use the datum from the stack in response to a pop command." (Emphasis added). The rejection of claim 21 under 35 USC 101 should be withdrawn at least for reasons similar to claim 1. Further, the Office Action states "As to the control logic, control logic is an abstract idea." This contention is respectfully traversed. The control logic, recited in claim 21, refers to a component of the stack module that responds to commands. Thus, the control logic is a physical component. See, e.g., Specification, page 12, lines 10-13, reference numeral 51 in Figure 4. Therefore, as recited in claim 21, control logic is not a non-functional

descriptive material. The rejection of claim 21 under 35 USC 101 should be withdrawn for this additional reason. Also, the rejection of claim 29 under 35 USC 101 should be withdrawn at least for reasons similar to claim 21 and the additional recitations that it contains.

Non-statutory double patenting

Claims 1, 2, 14, 21, 29, and 30 stand rejected on the grounds of non-statutory obviousness type double patenting as being unpatentable over U.S. Patent No. 6,631,462. A terminal disclaimer, in compliance with 37 CFR 1.321, is filed with this response to overcome the rejection. Accordingly, it is respectfully requested that the rejections on the grounds of non-statutory obviousness type double patenting be withdrawn.

35 USC 103(a)

Claims 1, 6-16, 19-25, and 27-30 stand rejected under 35 USC 103(a) as allegedly being unpatentable over LeBlanc et al. (US 5,542,070), hereinafter "LeBlanc," in view of Panwar et al. (US 5,838,988), hereinafter "Panwar." Claims 2 and 3 stand rejected under 35 USC 103(a) as allegedly being unpatentable over LeBlanc in view of Panwar and further in view of Drimak (US 3,889,243). Claims 4 and 5 stand rejected under 35 USC 103(a)

as allegedly being unpatentable over LeBlanc in view of Panwar, further in view of Drimak, and further in view of Picket et al. (US 5,968,169), hereinafter "Picket." Claims 17 and 18 stand rejected under 35 USC 103(a) as allegedly being unpatentable over LeBlanc in view of Panwar and further in view of Dangelo (US 5,946,487). Claim 26 stands rejected under 35 USC 103(a) as allegedly being unpatentable over LeBlanc in view of Panwar and further in view of Duncan (5,617,327). These rejections are respectfully traversed. The suggested combination of LeBlanc and Panwar does not disclose all the features of the claimed subject matter.

LeBlanc relates to programming of computer systems. See, e.g., LeBlanc, col. 1, lines 9, 10. Further LeBlanc describes a method for allowing a computer system to simulate a system. See, e.g., LeBlanc, col. 2, lines 12-14. The cited portion of the LeBlanc states:

> The inner interpreter then performs a doubly indirect function call to the C function xcolon, advancing the interpreter pointer to the next position in the thread, pointing to the reference ';'. Xcolon pushes the current value of IP onto the return stack, and then sets IP so it points to the beginning of the thread in the word 'u.' It then returns control to the inner interpreter. In effect, xcolon has performed a transfer of control from the thread test to the thread 'u,' in a manner analogous to a subroutine call. At the completion of execution of the thread 'u,' control can be returned to the thread test using the value saved on the return stack. The inner interpreter then

> consecutively executes the code for each of the words specified in the thread for 'u.' At the conclusion of the thread for u, the inner interpreter will execute the code associated with the reference to ';' - the C function xsemicolon. This function pops the top of the return stack, placing the return address back into IP." (Emphasis added). See, LeBlanc, col. 1, lines 7-23.

Thus, LeBlanc describes pushing the current value of IP onto the return stack and placing a return address back into IP by popping the top of the return stack. LeBlanc does not describe or suggest "pushing a datum onto a stack by a first hardware-controlled processing thread in a hardware-based multi-threaded processor," as recited in claim 1. The Office Action acknowledges that LeBlanc did not specifically show the hardware based multi-threaded processor as claimed. See, e.g., Office Action, page 7, paragraph 5. Further, the Office Action contends that Panwar teaches a hardware supported multi-threaded processor. Panwar describes microprocessor architecture providing precise state updates in an out-of-order machine. See, e.g., Panwar, col. 2, lines 24-27. The cited portion of Panwar states, "The present invention can be implemented in a processor having hardware support for multi-thread operation as shown in FIG. 6." See, Panwar, col. 12, lines 63-65. However, the suggested combination of LeBlanc and Panwar does not describe or suggest "to make available the datum for other hardware-controlled processing threads in the hardware-based

multi-threaded processor," as recited in claim 1. Thus, LeBlanc in view of Panwar describes or suggests all the features recited in claim 1. Further, LeBlanc, Panwar, Drimak, Picket, Dangelo, and Duncan, taken alone, or in any combination, do not describe or suggest the features of the subject matter as claimed. Therefore, a prima facie case of obviousness is not established. Accordingly, claim 1 is patentable. Claims 2-13 are also patentable at least for the same reasons and the additional recitations that they contain.

Claim 14, 21, 29, and 30 are also patentable for reasons similar to claim 1. Claims 15-20 are also patentable at least for the same reasons and the additional recitations that they contain. Claims 22-28 are also patentable at least for the same reasons and the additional recitations that they contain.

CONCLUSION

In view of the amendments and remarks herein, claims 1-30 are in condition for allowance and notice of allowance is respectfully requested. It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims)

that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

It is respectfully suggested for all of these reasons, that the current rejections are overcome, that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: May 14, 2007

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